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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,823	11/16/2001	Ameha Aklilu	RPS9 2001 0107	3066

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,823	AKLILU ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/16/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 36 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 36 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shinichi et al. [hereinafter as Shinichi], US Patent 6,523,133 B2.

5. As to claims 1, and 17 Shinichi discloses an information processing apparatus and method for reducing the boot time for a computer [col. 1, lines 37 – 41] comprising the steps of:

(a) supplying power to the computer [by external power supply, col. 2, lines 16 – 22, col. 5, lines 18 – 19, col. 8, lines 20 - 28];

(b) disabling a plurality of input/output (I/O) devices coupled to the computer [by detecting a preceding state system inherently disables I/o devices for restoring to that state and preventing regular booting][col. 2, lines 16 – 40, col. 3, lines 3 – 7, col. 5, lines 56 - 64];

(c) performing a boot process [inherent OS program] for the computer [col. 5, lines 39 – 43]; and

(d) placing the computer in a suspend to memory state [S3 state], wherein the steps (a) through (d) are performed before a user turns on [before user commands restoration of the state prevailed] the computer [col. 2, lines 16 – 67, col. 3, lines 3 – 30, col. 5, lines 18 - 63, col. 7, lines 46 – 56, col. 8, lines 20 – 28, fig. 23, 7 – 8, 13].

6. As to claims 11, and 27, Shinichi discloses an information processing apparatus and method for reducing the boot time for a computer [col. 1, lines 37 – 41] comprising the steps of:

(a) supplying power to the computer [by external power supply, col. 2, lines 16 – 22, col. 5, lines 18 – 19, col. 8, lines 20 - 28];

(b) determining [by checking activation flag] if the power is supplied to the computer when the computer is in a powered down state [S4] or a suspend to memory state [S3] [activation flag value indicating different conditions, col. 17, lines];

(c) booting the computer when the power is supplied to the computer when the computer is in a powered down state, wherein the booting step (c) comprises:

(c1) disabling a plurality of I/O devices coupled to the computer [by detecting a preceding state system inherently disables I/o devices for restoring to that state and preventing regular booting][col. 2, lines 16 – 40, col. 3, lines 3 – 7, col. 5, lines 56 - 64],

(c2) performing a boot process [inherent OS program] for the computer [col. 5, lines 39 – 43], and

(c3) placing the computer in the suspend to memory state [S3] [col. 2, lines 16 – 67, col. 3, lines 3 – 30, col. 5, lines 18 - 63, col. 7, lines 46 – 56, col. 8, lines 20 – 28, fig. 23, 7 – 8, 13]; and

(d) operating the computer in a wake state [S2] if the power [external power] is supplied to the computer when the computer is in the suspend to memory state [S3] [col. 17, lines 11 –67, col. 18, lines 1 – 50, col. 2, lines 16 – 67, col. 3, lines 3 – 30, col. 5, lines 18 - 63, col. 7, lines 46 – 56, col. 8, lines 20 – 28, fig. 23, 7 – 8, 13].

7. As to claim 33, Shinichi discloses a computer system comprising:

a. a plurality of I/O devices [fig.5]; and

b. a computer coupled to the plurality of I/O devices [fig. 5], the computer comprising:

(i) a BIOS [inherent for booting, col. 17, line 45],

(ii) a memory [col. 4, lines 63 – 67], and

(iii) an OS [operating system program, col. 4, lines56 – 58], wherein when power [external power] is supplied to the computer before a user turns on the computer, the BIOS disables the plurality of I/O devices and performs a boot process for the computer, and the OS places the computer in a suspend to memory state[col. 2, lines 16 – 67, col. 3, lines 3 – 30, col. 5, lines 18 - 63, col. 7, lines 46 – 56, col. 8, lines 20 – 28, col. 17, lines 13 – 18, fig. 23, 7 – 8, 13].

8. As to claims 2 – 3, and 18 – 19, Shinichi discloses supplying of power by plugging the computer into an AC outlet [by plugging supply line to external power supply AC outlet, col. 2, lines39, fig. 5 – 6] when the computer is in powered down state [hybernating state S4, fig. 2].

9. As to claims 4, 12, 20, 23, and 28, Shinichi discloses performing the boot process for computer by a basic input/Output system [BIOS] [col. 16, lines 1 – 3] and setting of flag [activation flag F is set] by BIOS [col. 16, lines 1 - 34].

10. As to claims 5, 21, 30, and 34, Shinichi discloses a setting of activation flag F in storage area of memory which is inherently have a registers too [col. 10, lines 44 – 55].

11. As to claims 6, 13, 22, 29, and 35 - 36, Shinichi discloses checking [detecting the activation flag F value] in storage register of memory for different scenario of state transition [col. 10, lines 48 – 55, col. 11, lines 30 – 36, col. 17, lines 13 – 53].

12. As to claims 7, and 23, Shinichi discloses S3 state [fig. 8].

13. As to claims 8, 14, 24, and 31, Shinichi discloses supplying power to the computer when the computer is in the suspend to memory state [S3][col. 6, lines 55 – 58]; resuming operation of an OS of the computer [col. 7, lines 46 – 56] ; checking a flag [activation flag F] by the OS, wherein the flag indicates whether or not the computer is being booted from a powered down state [S4][col. 13, lines 43 – 67]; enabling the plurality of I/O devices [inherently enabled during initialization] if the flag indicates that the computer is not being booted form the powered down state [during initial state S1, col.5, lines 43 – 49]; and operating the computer in a wake state [col.7, lines 46 – 50, col. 8, lines 20 - 28].

14. As to claims 9 – 10, 15 – 16, 25 – 26 and 32, Shinichi discloses to place computer in suspend to memory [S3] state and restoring it back to suspend state [S3] by manipulation start/stop switch [col. 2, lines 62 – 67, col. 3, lines 1 – 23, col. 6, lines 55 – 58, col. 8, lines 20 – 28, fig. 2, 3].

15. Prior Art not relied upon:

Please refer to the references listed on which are not relied upon in the claim the attached PT0-892 rejections detailed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 7:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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Nitin C. Patel
October 26, 2004